Power efficient analog circuit design: A tutorial overview

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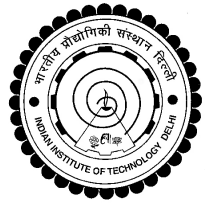
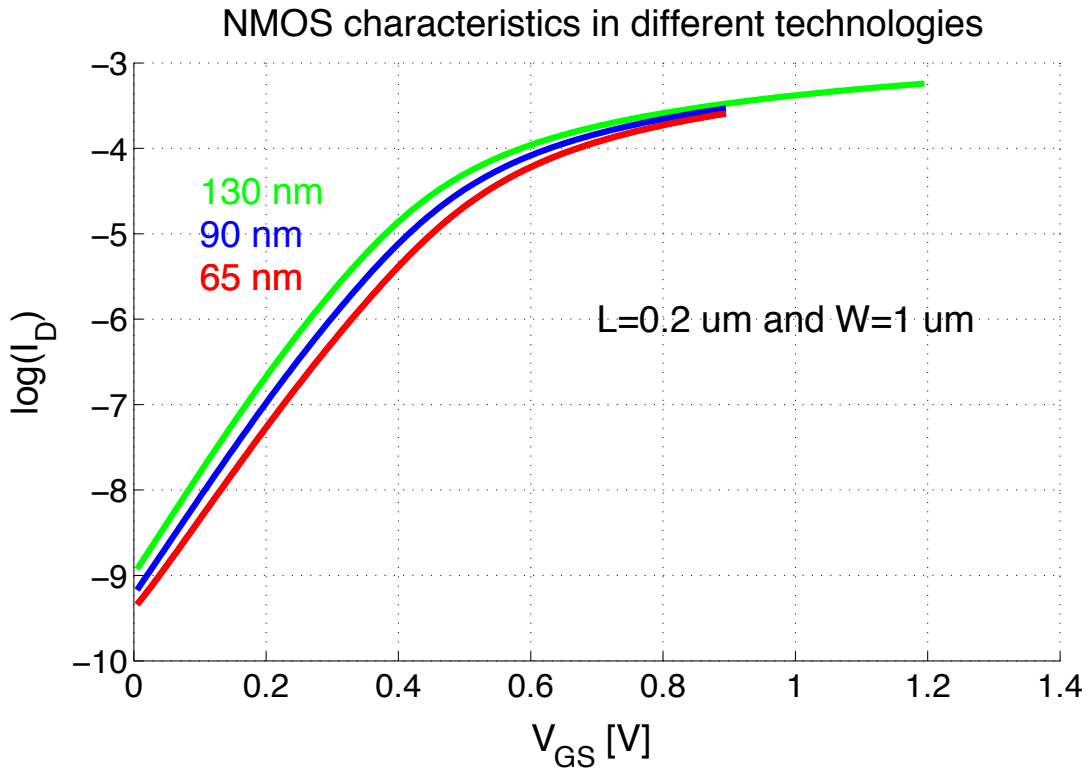
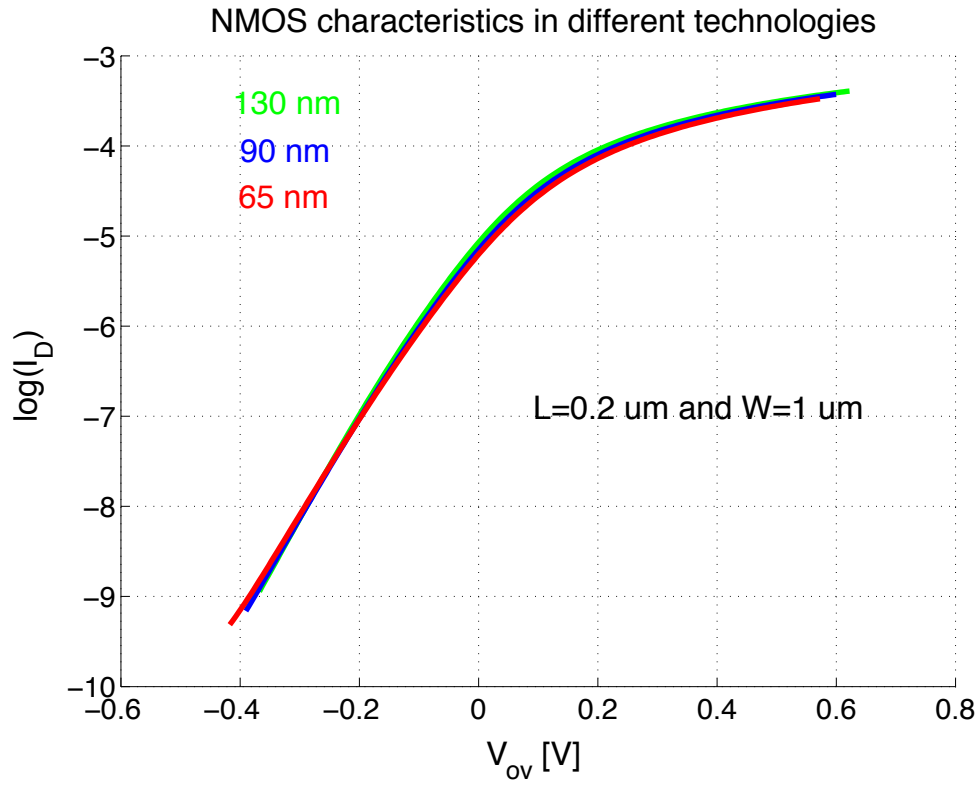


Review of MOSFET characteristics



- Sub-threshold, strong inversion and velocity saturation.
- For low power analog design, designers try to operate the transistor in sub-threshold region.

V_{ov} and low power



- $V_{ov} = V_{GS} - V_{th}$ is the parameter that the designers use extensively in their designs, in particular to fix the operating region of a transistor.

Short comings of V_{ov}

- In lower technologies fixing $V_{ov} = V_{GS} - V_{th}$ is a tedious job as the threshold voltage varies with every design parameter.
- Moreover in most of the analog circuits, current biasing is used rather than a voltage biasing.
- How to fix V_{ov} in current biasing schemes?
- Is there any current based parameter that serves the same objective as of V_{ov}?

$I_D - V_{ov}$ in different regions

Weak Inversion	I_D	=	$I_s e^{V_{GS}/(nkT/q)}$
Strong Inversion	I_D	=	$(KP/2n)(W/L)(V_{GS} - V_{th})^2$
Velocity saturation	I_D	=	$WC_{ox}\vartheta_{sat}(V_{GS} - V_{th})$

- In any region, I_D can be expressed as a product of two functions as follows.
- $I_D = f_1(C_{ox}, KP, n, W, ..).f_2(V_{GS})$
- f_1 is function of process parameters and f_2 is a function of V_{GS} only.

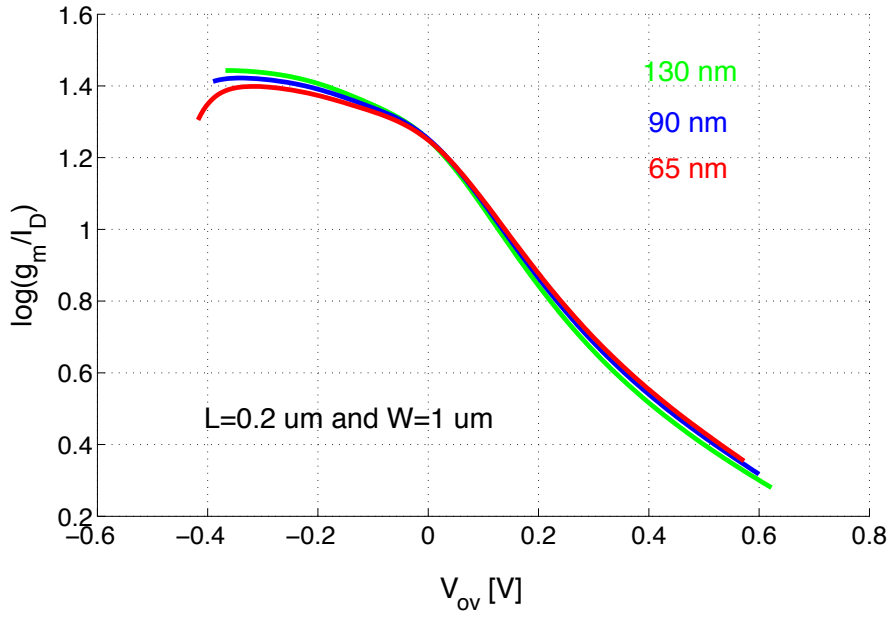
Transconductance and g_m/I_D

- Transconductance of a transistor is defined as follows.

$$\begin{aligned} g_m &= \partial I_D/\partial V_{GS} \\ &= f_1 \,.\, \partial f_2/\partial V_{GS} \\ &= I_D/f_2 \,.\, \partial f_2/\partial V_{GS} \end{aligned}$$

- Hence $g_m/I_D = (1/f_2).(\partial f_2/\partial V_{GS})$ is a function of voltages only.
- More interestingly, it is easy to see that f_2 and hence g_m/I_D are functions of V_{ov} only in the strong inversion and velocity saturation regions.

Invariance of (g_m/I_D) - V_{ov}

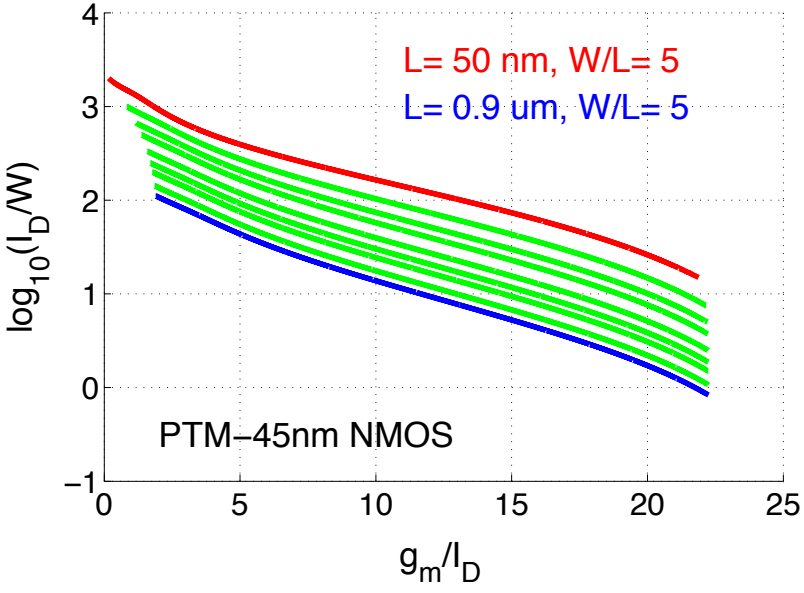


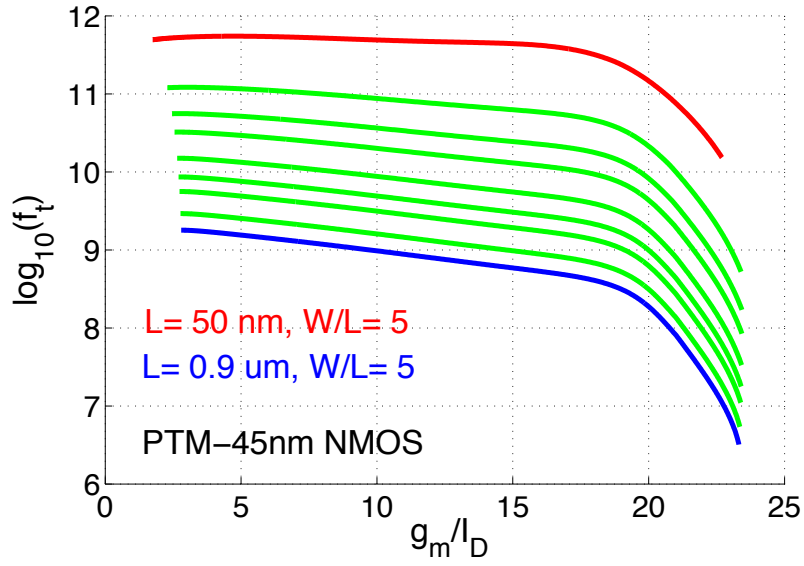
- There is a, technology independent, one to one relation between g_m/I_D and V_{ov} in the regions of interest.
- So lets replace V_{ov} with g_m/I_D as a design parameter in all the design equations or graphs.

Graph based design

- At lower technology nodes, there are no simple and accurate MOSFET models available for hand calculations.
- So the best way to design is to pre-generate a set of plots at different lengths and use these plots in the design rather than any analytical expression.
- Which plots to be pre-generated?

Set of plots to be used

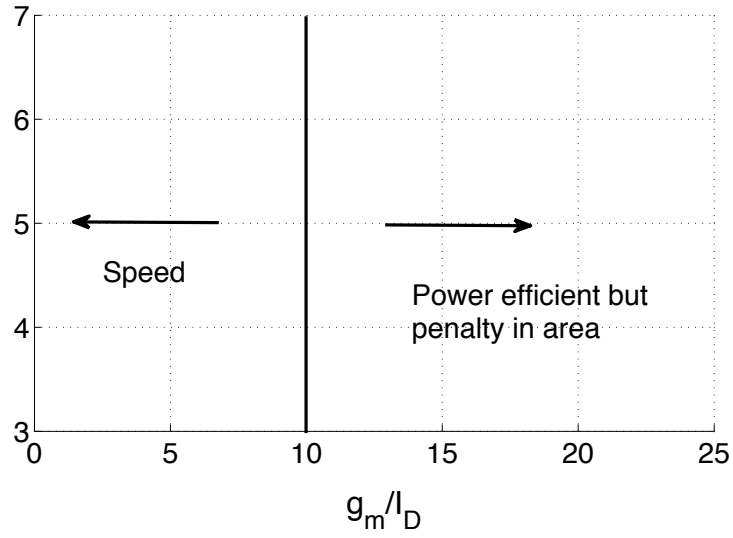




- Instead of $I_D - V_{ov}$ shown previously, we use the $(I_D/W) - (g_m/I_D)$.
- Instead of the $C_g - V_{GS}$ graph we use $f_t - (g_m/I_D)$ graph.

Few comments

- Larger the g_m/I_D ratio, more power efficient the circuit is.
- g_m/I_D of 10 is the optimum point where we get a compromise between speed, power and area. (This corresponds to V_{ov} = 0.2 V)



Few comments

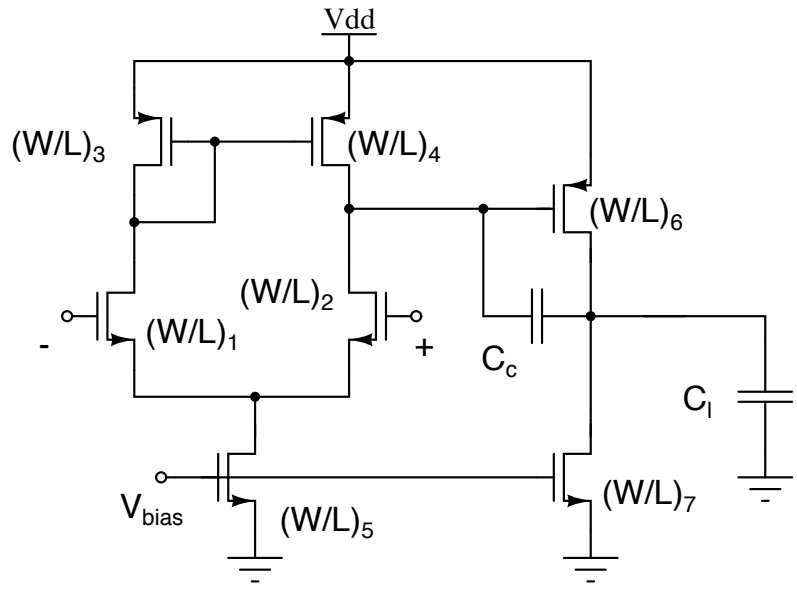
- We can't achieve the g_m/I_D more than 25. This is a fundamental limit that can be used to check the feasibility of the specifications for a particular architecture.
- V_{dsat} can be approximated as $2/(g_m/I_D)$ in the design of current sources/sinks.
- To get more r_{ds}, we have to increase the length.
- To get a particular GBW, we have to choose the length such that $f_t >>$ GBW.

Design procedure

- From the top level specifications, get the current flowing through each transistor and/or the trans conductance of the input transistor.
- Pick a length and a g_m/I_D to achieve a particular GBW (from the $f_t - (g_m/I_D)$ graph).
- From the chosen g_m/I_D, get the I_D value as g_m is known from the top level specifications.

- Now from the current density graph, note down the I_D/W value for the chosen set of g_m/I_D and length.
- Since we have I_D and I_D/W, the value of the width can be computed.
- Proceed in the similar lines for all other transistors.

Design example



- Let us design a Miller OTA with a GBW $\geq$ 200 MHZ with a load capacitance of 1 pF and a gain $\geq$ 50 dB and a PM of 60 deg. in 45 nm.

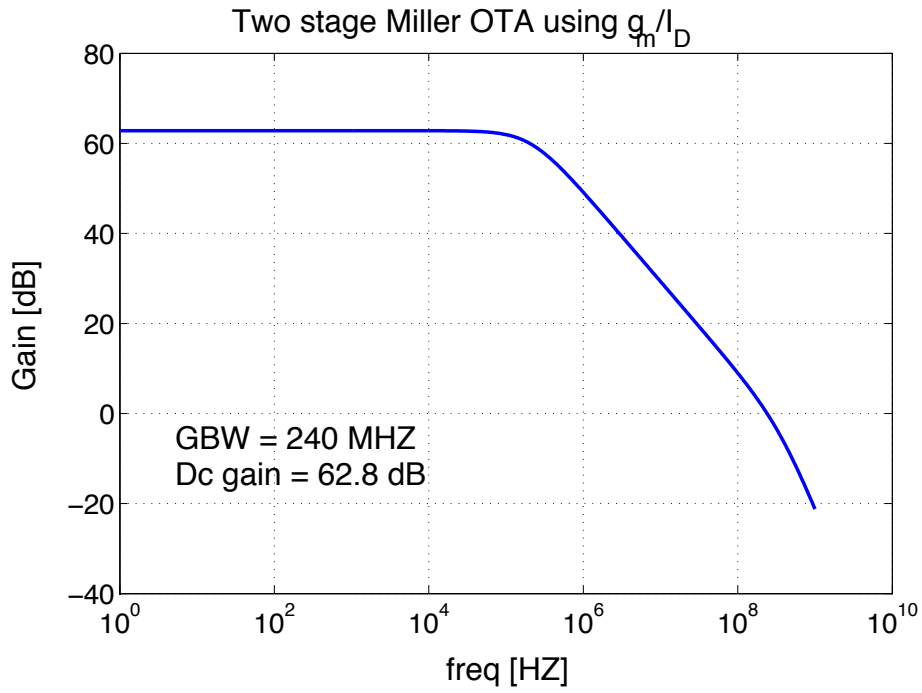
- For matching requirements, we have $(W/L)_1 = (W/L)_2$, $(W/L)_3 = (W/L)_4$ and $L_5 = L_7$.
- From the given specifications, $C_c \geq 0.22C_l$, $g_{m1} \geq 2\pi(GBW)C_c$, and $g_{m6} = 10g_{m1}$
- From the $f_t - (g_m/I_D)$ graph, we have decided to use the following lengths and g_m/I_D s.
- $L_1 = L_2 = 0.1\mu m$ and $g_m/I_D = 15$
- $L_3 = L_4 = 0.2\mu m$ and $L_5 = L_7 = 0.5\mu m$
- $L_6 = 0.1\mu m$ and $g_m/I_D = 10$

Simulated results

- Following widths are read from the current density plots.

  $W_1 = W_2 = 1.5\mu m$, $W_3 = W_4 = 4\mu m$, $W_5 = 3.5\mu m$,

  $W_7 = 17.5\mu m$ and $W_6 = 25\mu m$



Conclusion

- Reviewed the MOSFET characteristics at lower technology nodes.
- Introduced g_m/I_D as an alternative design variable to V_{ov}.
- Proposed a graphical approach as opposed an analytical approach.
- Just two plots and few thumb rules are all needed to carry out any analog design.
- Demonstrated a possible design methodology.