Revised Model Syllabus for Type II (incorporating system design courses)

CURRICULUM

It was decided to have 4 Core courses, 3 Core design laboratories and 4 Electives in addition to Seminars and Project. It was expected that a student put in about 40 hours of work per week. This includes about 20 hours of instruction/labs and 20 hours self-study.

The suggested distribution of the courses is as follows:
Semester I

S.No	Subject	Core/ Elective	No. of hours of Instruction per week
01	Semiconductor Devices	Core	3 hrs.
02.	Digital IC Design	Core	3 hrs.
03.	Analog IC Design	Core	3 hrs.
04.	Elective-I	Elective	3 hrs.
06.	Technical Communication	Elective	2 hrs.
07.	Design Laboratory (Digital and Analog)	Core	6 hrs.

Semester II

S.No	Subject	Core/ Elective	No. of hours of Instruction per week
08	System-on-Programmable Chip Design	Core	3 hrs.
09.	Elective-II	Elective	3 hrs.
10.	Elective-III	Elective	3 hrs.
11.	High Level Design Lab.	Core	6 hrs.
12.	System-on-Programmable Chip Design Lab.	Core	2hrs.
13.	Seminar	Core	2 hrs.
14.	Project	Core	8 hrs.

Semester III

S.No	Subject	Core/ Elective	No. of hours of Instruction per week
15.	Elective-IV	Elective	3 hrs.
16.	Project	Core	30 hrs.

Semester IV

S.No	Subject	Core/ Elective	No. of hours of Instruction per week
17.	Project	Core	36 hrs.

Elective Courses
The electives be grouped into two groups, one known as Programme Electives and the other known as General or Related Electives.

The following sets of electives are suggested in each of these categories:

Category I: Programme Electives
1.Digital Signal Processing
2.VLSI Systems Design
3.Embedded Systems & RTOS
4.Mixed Signal IC Design
5.VLSI Testing
6.RF IC Design
7.VLSI Technology

Category II: General or Related Electives
1.Low Power Design Techniques
2.Mapping Signal Processing Algorithms on DSP Architectures
3.MOS Device Modeling and Characterization
4.Architectural Design of IC's
5.High Speed system (board level) Design- (includes PCB design, thermal management, power supply)

Model Syllabus for Type –III

Electives can be chosen from a large number of courses offered by the institutes other than M. Tech in VLSI. However, the following additional sets of electives are suggested:

1. Embedded systems and RTOS
2. High Speed system (board level) Design- (includes PCB design, thermal management, power supply)- similar to course run by IISc
3. System-on-Programmable Chip Design (for Computer Science and Computer Architecture courses, requires programming/HDL core background)

Model Syllabus for Type -IV

Core Courses if not already covered

S. No	Subject	Core/ Elective	No. of hours of Instruction per week
01	SPICE	Core	3 hrs.
02.	Hardware Description Languages	Core	2 hrs.
03.	Design Lab (to cover both core courses)	Core	6 hrs.

Development of Model Syllabus for B.Tech / M.Tech oriented towards SoC/ System Designing and initiating M.Tech in VLSI / Embedded System Designing: Model Syllabus for B.Tech and M.Tech oriented towards System Designing / SoC would be developed. Institutions, particularly those who participated in SMDP-II, would be encouraged to start this program during the course of the project with approval from their competent authority. In addition to this, efforts would be made to initiate M.Tech in VLSI/embedded systems, within three years of commencement of the program, in the Participating Institutions which at present do not offer M. Tech courses in these areas. This will, however, require approval of their competent authority.

Syllabi for Core Courses

Course Title: **Semiconductor Devices**

Course Content:

Introduction

1. *Basic Semiconductor Physics*

   Crystal lattice, energy band model, density of states, distribution statistics – Maxwell-Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, - drift, diffusion, thermionic emission, and tunneling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger, radiative, and surface.

2. *Junctions*

   p-n junctions – fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristic, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions – fabrication, Schottky barriers, rectifying ad ohmic contacts, I-V characteristics.

3. *MOS Capacitors and MOSFETs (~40%)*

   The MOS capacitor – fabrication, surface charge –accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; the MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristic, second-order effects – Velocity saturation, short-channel effects, charge

sharing model, hot-carrier effects, gate tunneling; subthreshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model (UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel IGFET model (BSIM).

4. *MOSFETs and HEMTs (~10%)*

   MESFETs –fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, backgating effect, SPICE model; HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, SPICE model.

5. *BJPs and HBTs (~20%)*

   BJTs – fabrication, basic operation, minority carrier distributions and terminal currents, I-V characteristic, switching, second-order effects – base narrowing, avalanche multiplication, high-injection, emitter crowding, Kirk effect, etc.; breakdown, high-frequency response, Gummel-Poon model, SPICE model; HBTs: - fabrication, basic operation, technological aspects, I-V characteristics, SPICE model.

References

1. Ben G. Streetman, Solid State Electronic Devices, Prentice Hall, 1997.
2. Richard S. Muller and Theodore I. Kamins, Device Electronics for Integrated Circuits, John Wiley, 1986.

Course Title: **Digital IC Design**

Course Content:

- Brief introduction to MOS transistor models and SPICE parameters; process parameters and design rules
- Requirements for restoring logic; design of static CMOS, nMOS and BiCMOS inverters
- Calculation of noise margins, power dissipation and gate delays; discussion of design trade offs

- Design of combinational circuits using static CMOS, pseudo-nMOS and DCVSL and DSL logic gates
- Design of combinational circuits using pass transistors and transmission gates
    - CPL, DPTL and swing restored pass transistor logic styles
- Design of synchronous sequential circuits
    - Two phase clocks, design of flip-flops and latches, design and implementation of state machines
- Dynamic logic circuits
    - Basic concepts, logic styles including np, Domino, NORA and TSPC logic, problems due to charge sharing and race conditions
- Design of IO buffers and on chip load drivers; PLL, clock generation and clock buffering; design of memory cells and sense amplifiers
- Design of adders
    - Ripple carry, Manchester carry, carry look ahead, carry select and carry save
- Design of multipliers (for unsigned and signed)
    - sequential, parallel, carry save, Booth multipliers; Wallace tree structures
- Implementation using residue number and distributed arithmetic
- Design of shifters and floating point arithmetic units

Text Books

1. J.M.Rabaey - Digital Integrated Circuits - A Design perspective
2. N.Weste and K.Eshraghian - Principles of CMOS VLSI Design - A Systems perspective

References

1. K.Martin - Digital integrated circuit design
2. J.Kuo and J.Lou - Low voltage CMOS VLSI circuits

3. S.Y.Kung - VLSI Array processors
4. W.Wolf - Modern VLSI Design

Course Title: **Analog IC Design**

Course Content:

- *Basic Analog Building Blocks*

  - Switches
  - Active Resistors
  - Current and Voltage sources
  - Current Mirrors
  - Current and voltage references
  - Voltage regulators

- *Amplifiers*

  - Basic Amplifiers
  - Differential Amplifier
  - Cascode Amplifiers
  - High Gain Amplifier Structure
  - Amplifier design

- *Operational Amplifiers*

  - Operational Amplifier characteristics
  - Basic Op.Amp circuits
  - Frequency response and compensation
  - Noise sources in Op-Amps
  - Op-Amp design including Biasing circuits
  - High performance Op-Amps

- *Comparators*

  - Single stage comparators
  - Two stage comparator
  - Comparators with Hysterisis
  - Auto zero techniques

References

1. “Analog MOS Integrated Circuits for Signal Processing”, Roubic Gregorian and Gabor C. Temes, John Wiley & Sons, 1986.
2. “VLSI Design Techniques for Analog and Digital Circuits”, Randall Geiger, Phillip E. Allen and Noel Stradder, McGraw Hill International Edition, McGraw Hill.
3. “CMOS Analog Circuit Design” Phillip E. Allen and Douglas R. Holberg.

Course Title: **Design Laboratory**

Course Content:

- Use of SPICE for circuit design.
- Logic design using IRSIM. Layout design using MAGIC or Tanner Tools.
- Circuit extraction from layout and verification by simulation of extracted circuits.
- Digital circuit design using VHDL/Verilog, Design using FPGAs.

References

1. SPICE manual
2. IRSIM manual
3. MAGIC manual
4. Xilinx Corporation, “FPGA technology for Nineties” Xilinx Handbook, 1992.

Course Title: **System-on-Programmable-Chip Design**

Course Content:

Theory:

1. Introduction

Driving Forces for SoC - Components of SoC - Design flow of SoC - Hardware/Software nature of SoC - Design Trade-offs - SoC Applications

2. System-level Design

Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom-Designed processors- on-chip memory.

3. Interconnection

On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, CoreConnect, Wishbone, Avalon - Network-on-chip: Architecture-topologies-switching strategies - routing algorithms - flow control, Quality-of-Service- Reconfigurability in communication architectures.

4. IP based system design

Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse - IP integration - IP evaluation on FPGA prototypes.

5. SOC implementation

Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design.

6. SOC testing

Manufacturing test of SoC: Core layer, system layer, application layer-P1500 Wrapper Standardization-SoC Test Automation (STAT).

Lab:
(Can be designed around either Xilinx Microblaze / Altera NIOS / OpenRISC + Wishbone)
Implementation of basic SoPC using tools; interfacing with peripherals; creation of custom peripherals using HDL; enhancement of instruction set with custom instructions; optimizing system architecture through choice of processor enhancements – architecture exploration

References:

1. Michael J.Flynn, Wayne Luk, “Computer system Design: System-on-Chip”, Wiley-India, 2012.
2. Sudeep Pasricha, Nikil Dutt, “On Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann Publishers, 2008.
3. W.H.Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Elsevier, 2008.

4. Patrick Schaumont “A Practical Introduction to Hardware/Software Co-design”, 2nd Edition, Springer, 2012.
5. Lin, Y-L.S. (ed.), “Essential issues in SOC design: designing complex systems-on-chip. Springer, 2006.
6. Wayne Wolf, “Modern VLSI Design: IP Based Design”, Prentice-Hall India, Fourth edition, 2009.

Course Title: **High level Design Lab**

Course Content:

- Experiments related to language semantics
    - Time Control: delay operator, event control.
    - Assignment Types: procedural, blocking, non-blocking, continuous.
    - Delay through combinational logic and nets
- Behavioural Coding (examples and problems)
- Structural Coding (examples and problems)
- RT-Level Coding (examples and problems)
- Mixed-Level Coding (examples and problems)
- Coding of state machines and sequential logic
- Coding of test benches
- Coding style for synthesis
- Entering design constraints and synthesis using "FPGA Express"
    - Generating timing reports; CLB/gate usage reports; Identifying suitableFPGA device (Xilinix) for design implementation.
- A mini-project example and suggestions for mini-project topics.

References

G. De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994.

P. Kurup and T. Abbasi, Logic Synthesis Using Synopsys, Second Edition, Kluwer, 1996.

J. Bhasker, A VHDL Primer, Third Edition, Prentice-Hall, 1999.

Z. Navabi, Verilog Digital System Design, McGraw-Hill, 1999.

S. Palnitkar, Verilog HDL : A Guide to Digital Design and Synthesis, Prentice-Hall, 1996.

Course Title: **Hardware Description Languages**

Course Content:

Foundations and Background

- Introduction to VLSI CAD
- Basic Concepts in Algorithms
- Graph Algorithms
- Linear, Integer and Nonlinear Programming
- Submodular functions in Combinatorial Optimization
- Probablistic Techniques for solving Large Problems

Combinatorial Problems in VLSI CAD

- Netlist Partitioning
- Placement, Assignment and Floorplanning
- Global Routing
- Detailed Routing
- Compaction

Additional topics

- Binary Decision Diagrams and their application to verification of digital ICs.
- Two and multi-level minimization for synthesis.
- Delay models and static timing analysis.
- Basic circuit simulation – matrix formulation, integration techniques, nonlinear systems.
- Interconnect issues – Model Order Reduction methods, crosstalk and inductance problems.

References

Electronic Circuit and System Simulation Methods – Lawrence Pileggi, Chandu Visweswaraiah and Ron Rohrer, McGraw-Hill, 1995.

Synthesis and Optimization of Digital Circuits – Giovanni DeMicheli , McGraw-Hill, 1994.

"Combinatorial Algorithms for Integrated Circuit Layout", Thomas Lengauer, John Wiley and Sons, 1990.

"Linear Programming", Vasek Chvatal, W. H. Freeman and Company, New York, 1983.

"Introduction to Algorithms", T. Cormen, C. Leicerson and R. Rivest, MIT Press, 1993.

"Combinatorial Optimization: Algorithms and Complexity" C. Papadimitriou and K. Steiglits, Prentice-Hall, Englewood Cliffs, N. J., 1982.

Laboratory work

1. Use of LEDA (Library of Efficient Data Structures and Algorithms) for implementing algorithms.
2. Exercises in formulation and solutions of VLSI CAD problems and optimization problems.

Syllabi for Electives

Course Title: **Digital Signal Processing**

Course Content

Discrete-Time Signals and systems: Basic sequences and sequence operations. Linear time invariant systems. Causality and stability. Linear constant coefficient difference equations. Discrete-time Fourier transform and its properties. Convolution and modulation theorems.

Z-Transform: Properties of the region of convergence. Inverse *z*-transforms. *z*-transform properties. Sampling of Continuous-time Signals: Periodic sampling. Frequency domain representation of sampling. Reconstruction of a band limited signal from its samples. Changing the sampling rate using discrete time processing. Multi-rate signal processing.

Transform Analysis of LTI Systems: Frequency response of LTI systems. Relationship between magnitude and phase. All-pass systems. Minimum phase systems, Generalised linear phase systems.

Structures of Discrete-time Systems: Signal flow graph representation of linear constant coefficient difference equations. Basic IIR structures. Transposed forms. Basic structures for FIR systems. Overview of finite-precision numerical effects.

Discrete Fourier Transforms: Representation of periodic sequences: discrete Fourier series and its properties. Fourier transform of periodic signals. Sampling the Fourier transform. Fourier representation of finite duration sequences: the discrete Fourier transform and its properties. Circular convolution, linear convolution using DFT.

Computation of the Discrete Fourier Transform: Efficient computation of the DFT. Goertzel algorithm. Decimation-in-time FFT and decimation-in-frequency FFT algorithms. In place computation. Alternate forms.

Text Book:

1. A.V. Oppenheim and R.W. Schaefer with T.R. Buck, "Discrete Time Signal Processing", 2nd Ed., Pearson Education Asia Pvt. Ltd., 2000.

Reference:

1. S. K. Mitra, "Digital Signal Processing – A Computer Based Approach", 2nd Ed., Tata Mc-Graw Hill, 2003.

Course Title: **VLSI Systems Design**

Course Content:

Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI chips; CISC Instruction-set implementation and RT-Level optimization through hardware flow-charting (without/with pipelining concepts); Microprogramming approaches for implementation of control part of the processor; Handling of Instruction boundary interrupts, Immediate interrupts and traps in processors; Pipelined implementation of RISC Instruction Sets; Benefits and problems of pipelined execution; Hazards of various types and pipeline stalling; Scheduling (static and dynamic) and forwarding to reduce/minimize pipeline stalls; Implementation of DSP Instruction sets; Programmable and function specific architectures; Synthesis of DSP architectures; Scheduling and resource allocation for DSP architectures; Design of processing elements; Conventional, residue number, cordic and distributed arithmetic architectures; Issues in the design and implementation of Instruction sets for special applications (optimizing the H/W – S/W interface);

Different abstraction levels in VLSI design; Design flow as a succession of translations among different abstraction levels; Gajski's Y-Chart; Need for manual designing to move to higher levels of abstraction with automatic translation at lower levels of abstraction; Need to model and validate the design at higher-levels of abstraction and the necessity of

HDLs that encompass several levels of design abstraction in their scope; VHDL hardware description language: introduction and detail; Verilog hardware description language: introduction and detail; Design flow for VHDL/Verilog based RTL/logic synthesis and behavioural synthesis approaches.

Course Title: **Embedded Systems& RTOS**

Course Content:

- Software:
  - Real-time models;
  - periodic/aperiodic tasks;
  - resource sharing
- RTOS:
  - basic OS functions;
  - task scheduling, prioritization;
  - inter-task communications; interrupts, semaphores;
  - event-driven systems
- Processing and communication:
  - system components;
  - interconnects;
  - bus architectures;
  - communication protocols;
  - microcontroller and FPGA architectures and instruction sets;
  - low-power design
- Hardware:
  - models of hardware – FSM, controller, micro-programmed etc.;
  - architecture synthesis
  - design space exploration

Lab:

- To be structured around available sensor nodes or similar platform for cooperative functioning of multiple nodes; example: Wireless / Bluetooth Motes
- FPGA platform: exploration of architectures; custom computing machines

References

1. Peter Marwedel: *Embedded System Design*

2. *W. Wolf. Computers as components: principles of embedded computing system design. Morgan Kaufmann, 2012.*
3. High-Performance VLSI Signal Processing : Innovative Architecture and Algorithms, Vol. 1 by K.J.Ray Liu and K.Yao, IEEE Press, 1998.

Course Title: **Mixed Signal IC Design**

Course Content:

- *Building blocks for CMOS amplifiers*: design of current mirrors, differential amplifiers.

- *CMOS operational transconductance amplifiers*: design of single ended telescopic cascode, folded cascode and two-stage amplifiers.

- *Frequency compensation schemes:* Miller compensation, Ahuja compensation and Nested-Miller compensation.

- Design of fully differential amplifiers, discussion of common mode feedback circuits.

- Switched capacitor circuits, design of switched capacitor amplifiers and integrators, effect of opamp finite gain, bandwidth and offset, circuit techniques for reducing effects of opamp imperfections, switches and charge injection and clock feed-through effects.

- Design of sample and holds and comparators.

- Fundamentals of data converters; Nyquist rate A/D converters (Flash, interpolating, folding flash, SAR and pipelined architectures); Nyquist rate D/A converters - voltage, current and charge mode converters, hybrid and segmented converters); Oversampled A/D and D/A converters.

- Design of PLL's and DLL's and frequency synthesizers.

Text books

1. R. Gregorian and Temes - Analog MOS integrated circuits for signal processing
2. R.Gregorian - Introduction to CMOS opamps and comparators.
3. D.Johns and K.Martin - Analog integrated circuit design

References

1. B.Razavi - Monolithic Phase-locked loops and clock recovery circuits: Theory and design.

Course Title: **VLSI Testing**

Course Content:

- Introduction and Elementary Testing Concepts
- Test Generation for General Combinational Circuits
- Test Generation for PLAs and Sequential Circuits
- Random Pattern Testing
- Logic Level Simulation
- Built in Self Testing
- Delay Fault Testing
- Memory Testing
- Design for Testability

Course Title: **RF IC Design**

Course Content:

Distortion and noise in amplifiers - dynamic range - Scattering parameters - radio receiver architectures -specification of individual blocks from top level specifications - analysis and modeling of on-chip passive elements - circuit biasing techniques - low noise amplifiers - variable gain amplifiers - mixers filters – received signal strength indicators -power amplifiers and linearization - RF measurement basics.

References

1. Thomas Lee - The design of CMOS RF ICs, Oxford University Press, 1997.

2. Behzad Razavi : RF Microelectronics, Prentice Hall, 1999.

Course Title: **VLSI Technology**

Course Content:

General Overview of current status of VLSI Technology

- Interaction between Technology and Design
- Interaction between Physics and Technology
- Limits of Technology

Environment for Integrated Circuits Manufacture

- Clean Rooms and Wafer cleaning procedures.
- Technology details of the Laboratory.

Unit- Processes in Fabrication

- Oxidation, Diffusion, Ion Implantation, Etching and Deposition techniques.
- Characterization of Processes.

Lithography and Mask generation techniques

- Advanced Unit-Processors for ULSI Circuit Technologies.
- Use of RTP
- Plasma processes in the fabrication in the fabrication of circuits.

Basic Bipolar process Technologies.

NMOS Technology

- Mask sequence based fabrication process for NMOS transistors.
- Silicon Gate and Metal Gate Technologies.
- Limitations of NMOS Technology.

CMOS Technology

- Process Sequence for CMOS Technology.
- Advanced CMOS Processes.

"Design – Rules" for NMOS and CMOS Technologies as "Constraints" for Layouts.

Process Simulation

- Use of SUPREM-IV ans STEP Simulators for process Design.
- Some Examples of actual technologies.

References

(1) VLSI Fabrication principles by S.K. Ghandhi; John Wiley Inc., New York, 1983
(2) VLSI Technology by S.M. Sze; 2nd Edition, McGraw Hill Co. Inc., New York, 1988
(3) VLSI Technology by C. Y. Chang and S. M. Sze; McGraw Hill Co. Inc., New York, 1996

Course Title: **Low Power Design Techniques**

1. Introduction; Power Dissipation in CMOS MOSFETs.

2. Power Estimation.

3. Design of Low-Power CMOS Circuits.

4. Low-Power SRAM/DRAM Design.

5. Software Design for Low Power.

TEXT BOOKS:

1. J. B. Kuo and J-H. Lou, *Low-Voltage CMOS VLSI Circuits*, Wiley, 1999.
2. K. Roy and S. C. Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley, 2000.

REFERENCE BOOKS:

1. A. P. Chandrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*, Kluwer, 1995.
2. A. P. Chandrakasan and R. W. Broderson, *Low-Power CMOS Design*, IEEE Press, 1998.
3. E. Sanchez-Sinencio and A. G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed Signal Circuits*, IEEE Press, 1999.
4. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson, 2003.

Course Title: **Mapping Signal processing algorithms on DSP architectures**

1. Firmware Development versus Architecture

- DSP development platforms
- C compiler
- Impact of C on architecture and vice versa
- Extensions to C, DSP-C
- Simulation Technologies, program verification
- Debug and emulation

4. DSP Classification and Benchmarking

- Benchmarking, MIPS, BDTi, EEMBC
- More than MIPS: power, code density, …
- Impact of architecture on performance
- Comparison of example architectures (ADI, Philips R.E.A.L., TI C55/C6x)

5. Multi-core DSP design

- Inter-processor communication
- Communication channels
- Firmware partitioning problems
- Debug and Emulation concepts

6. Future Developments

- Trend: towards higher performance?
- Trend: merge microcontrollers with DSPs?
- Trend: time-to-market: do we need floating point, C hardware

References

1. Real-Time Signal Processing Design and Implementation of Signal Processing Systems by J.G.Ackenhausen, IEEE Press+Prentice Hall, 2000.
2. VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis by V.K.Madisetti, IEEE Press+Butterworth-Heinemann, 1998.

3. High Performance VLSI Signal Processing: Systems Design and application, Vol.2 by K.J.Ray Liu and K.Yao, IEEE Press, 1998.

Course Title: **MOS Device Modeling and Characterization**

Course Content:

- *2-terminal MOS device:* threshold voltage modeling (ideal case as well as taking into account the effects of Q_f, Φ_{ms} and $D_{it.}$); C-V characteristics (ideal case as well as taking into account the effects of Q_f, Q_m and D_{it}); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Q_f, Q_m and D_{it})

- *4-terminal MOSFET:* threshold voltage (considering the substrate bias); above threshold I-V modeling (SPICE level 1,2,3 and 4); sub-threshold current model; scaling; effect of threshold tailoring implant (analytical modeling of threshold voltage using box approximation); buried channel MOSFET; short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

  SOI MOSFET: basic structure; threshold voltage modeling

  Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics

References

1. D.G.Ong , "Modern MOS Technology: Processes, Devices and Design", McGraw Hill, 1984.
2. Y.Taur and T.H.Ning, "Fundamentals of modern VLSI Devices" Cambridge Univ. Press, 1998.
3. S.M.Sze, "Physics of Semiconductor Devices" Wiley,1981.

Course Title: **Architectural Design of ICs**

Course Content

Introduction; General design methodologies; Datapath synthesis; mapping algorithms into architectures; Control strategies; concepts of system analysis; hardware implementation of various control structures; Microprogram control techniques; implementation of simple and nested subroutine calls; timing considerations; worst case system speed calculation; pipelined and parallel architectures; latency and throughput; dependency and dataflow; fault tolerance; fault-tolerant architectures.

Course Title: **High Speed System Design**

Theory

Course Content:

1. Transmission line theory (basics)

crosstalk and nonideal effects; signal integrity: impact of packages, vias, traces, connectors; non-ideal return current paths, high frequency power delivery, simultaneous switching noise; system-level timing analysis and budgeting; methodologies for design of high speed buses; radiated emissions and minimizing system noise;

Practical aspects of measurement at high frequencies; high speed oscilloscopes and logic analyzers

2. Printed Circuit Board

Anatomy, CAD tools for PCB design, Standard fabrication, Microvia Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation Cooling requirements.

3. Reliability

Basic concepts, Environmental interactions. Thermal mismatch and fatigue failures thermo mechanically induced electrically induced chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.

4. IC packaging

Requirements and properties; materials and substrates; wire-bonding; chip and wafer-level packaging; impact on reliability and testability

Lab:
Demonstration of high speed signal distortion effects; crosstalk; eye diagrams
Design: large design project on implementing multi-layer PCB and testing

References:

- "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", Stephen H. Hall, Garrett W. Hall, James A. McCall, August 2000, Wiley-IEEE Press
- Tummala, Rao R., Fundamentals of Microsystems Packaging, McGraw Hill, 2001
- R.G. Kaduskar and V.B.Baru, Electronic Product design, Wiley India, 2011